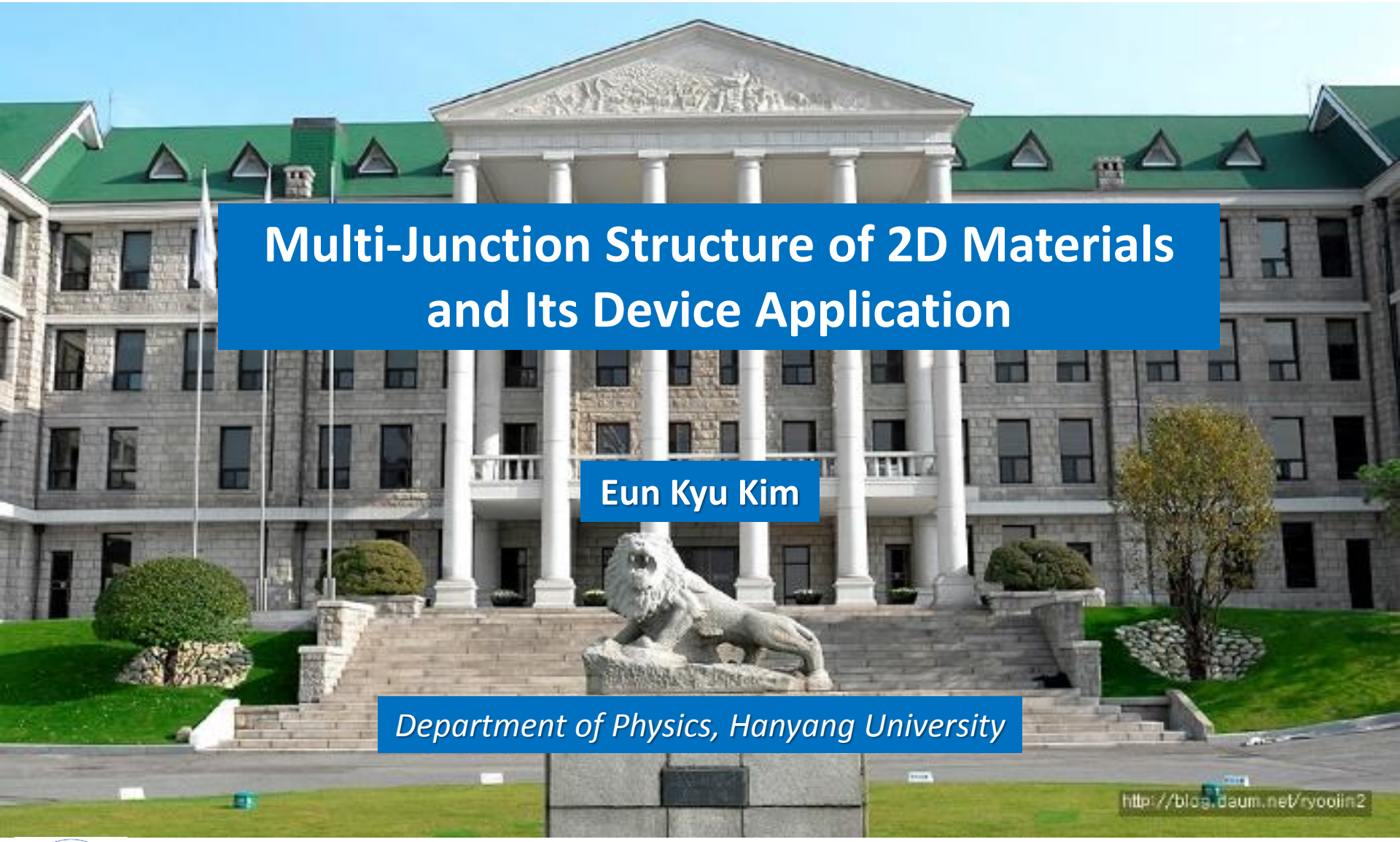


Multi-Junction Structure of 2D Materials and Its Device Application

Eun Kyu Kim

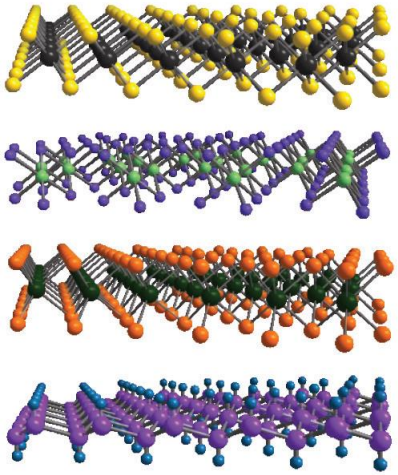
Department of Physics, Hanyang University

Contents

- ✓ A brief introduction; 2D materials and properties
- ✓ 2D and TMD materials transistor technologies
  - Interface engineering for MoS_2 FET
  - MGr-embedded memory devices
  - SnS_2/hBN TFT with broadband photoresponse
  - A new conceptual device, CARRISTOR
- ✓ Summary

Advantages of 2D materials for transistor

General formula: MX_2

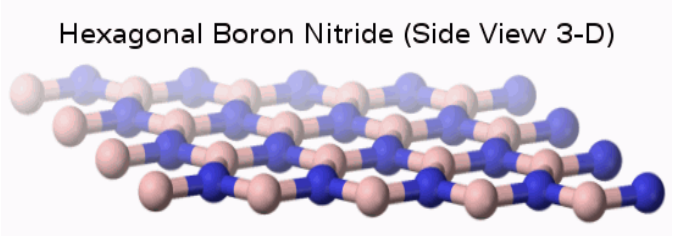


For example, **MoS_2**

Band gap: 1.2 eV (bulk, indirect); 1.8 eV (monolayer, direct)
Carrier mobility: 10-500 cm^2/Vs
Current on/off ratio: see below
Young's Modules: 200-300 Gpa
Strain limit: 23% (experiment)

- It is accessible on plastic substrate
- No dangling surface bonds
- Abundant material library

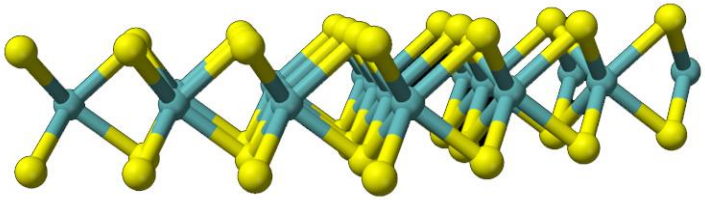
▪ hBN tunnel barrier



- Band gap: 5 eV
- Dielectric constant: 3-4
- Breakdown strength: 8 MV/cm

hBN is a perfect substrate without pinholes, ideal for tunnel barrier construction.

▪ WS_2 Channel material

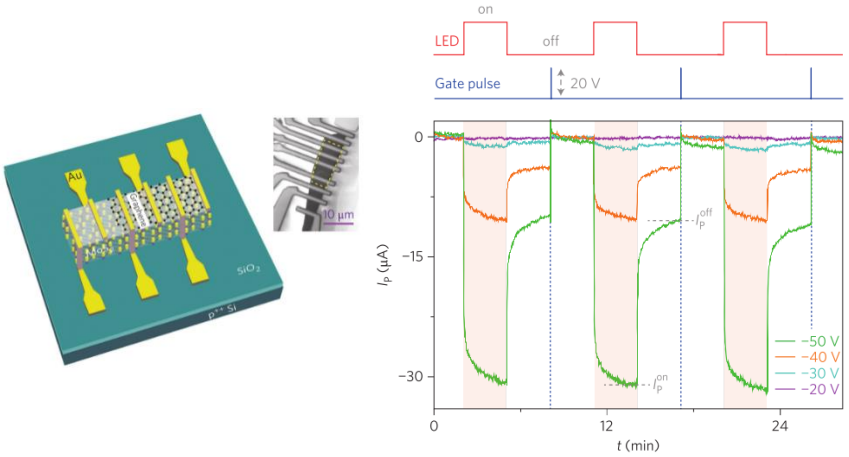


- Band gap: 1.3 eV (bulk, indirect)
- Electron affinity: 4.0-4.4 eV

It is theoretically predicted to have the lightest effective mass, a high thermal stability and a high chemical stability.

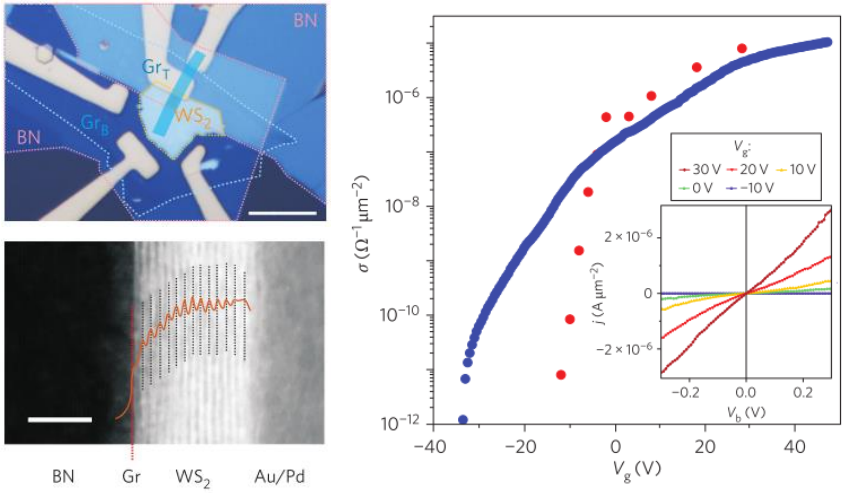
Demonstration of various functional devices

- **Graphene/MoS_2 optoelectronic switches**



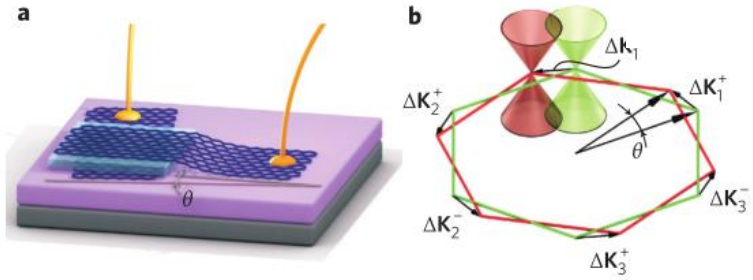
Roy *et al*. Nat. Nanotechnol. 8, 826 (2013)

- **WS_2 vertical tunneling transistor**

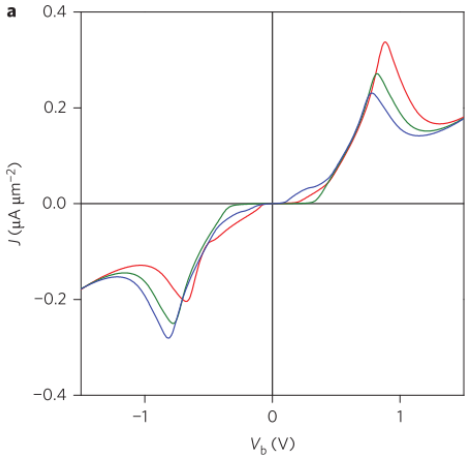


Georgiou *et al*. Nat. Nanotechnol. 8, 100 (2013)

- **Graphene/hBN/graphene resonant tunneling transistor**



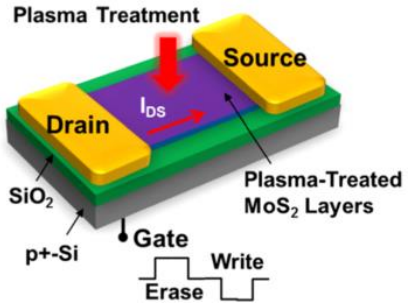
Mishchenko *et al*. Nat. Nanotechnol. 9, 808 (2014)

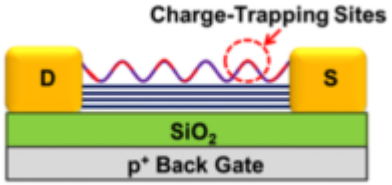


Floating-gate for memory cells

Various type of charge-confining layers

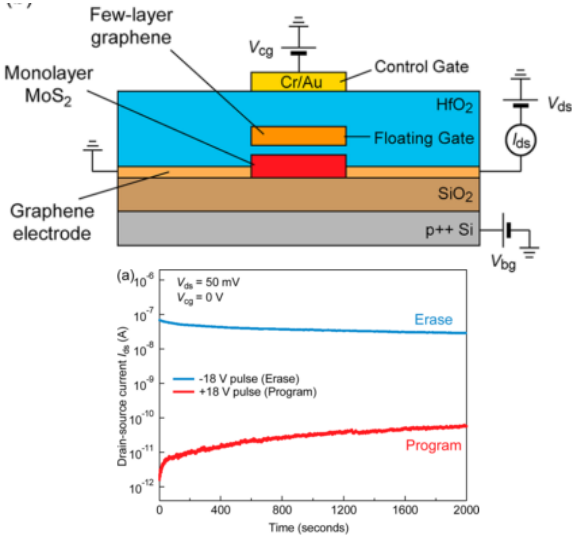
Plasma induced defect traps





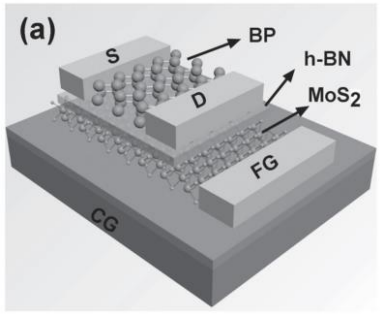
M. Chen et. al, ACS nano, 8, 4023-4032 (2014)

Few-layer graphene



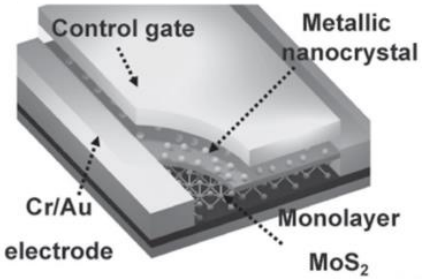
S. Bertolazzi et. al, ACS nano, 7, 3246-3252 (2013)

MoS_2



D. Li et. al, Adv. Funct. Mater. 25, 7360 (2015)

Metal nanoparticles



Wang et al. Small, 11, 208-213 (2014)

- By applying plasma treatment, the charge-trapping sites can be intentionally introduced.
  → then, the configuration of the device does not have floating-gate.
- The charge-confining layer could be graphene, MoS_2 itself, metallic nanoparticles and hafnium oxide etc.

TMDs transistor technologies

I. Interface engineering for MoS_2 FET

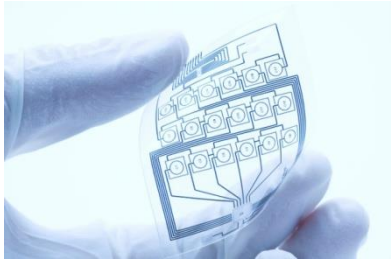
(1) Bridge channel MoS_2 FET, *Nanoscale* 7, 17556-17562 *(*2015)

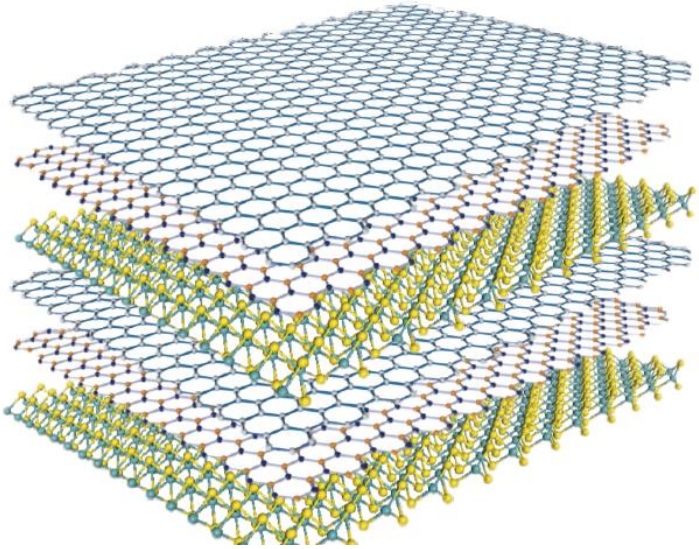
(2) Graphene/MoS_2 heterostructured FET, *Scientific Reports* 5, 13743 (2015)

II. MGr-embedded memory devices, *Nano Research* 9, 2319-2326 *(*2016)

III. Locally gated SnS_2/hBN TFT, *Scientific Reports 8*, 10585 (2018)

IV. A new conceptual device; CARRISTOR, *Science Advances* 3, e1602726 (2017)

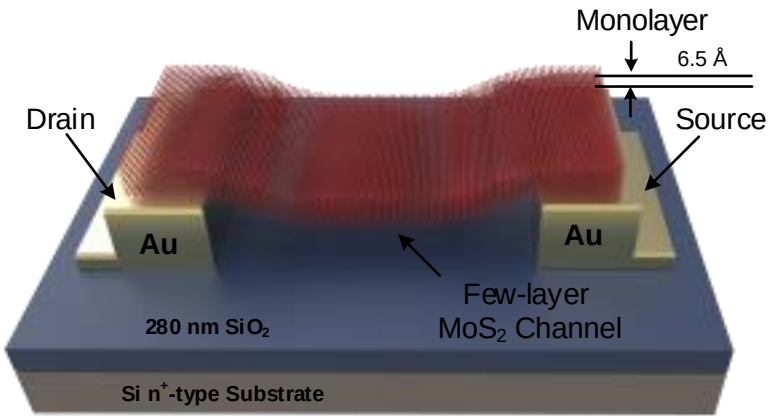




Tremendous opportunities for layer-by-layer stacking of electronic devices…

I. Interface engineering for MoS_2 FETs

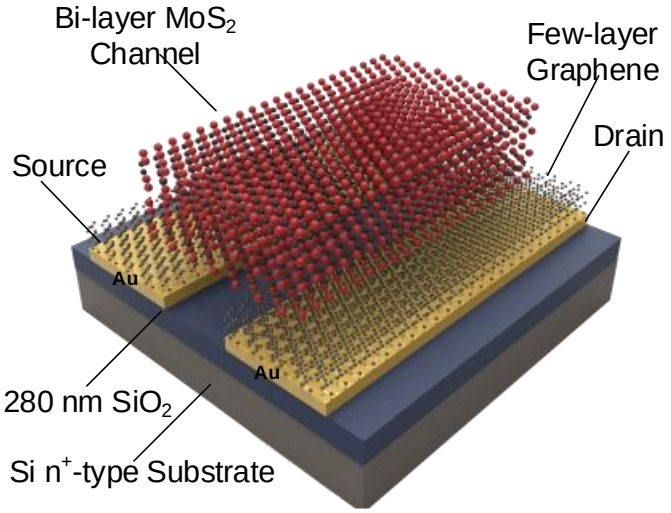
Bridge-channel MoS_2 FET



MoS_2/Vacuum interface

D. Qiu, D. U. Lee, C.-S. Park, K. S. Lee, and E. K. Kim, *Nanoscale* 7, 17556 (2015)

Graphene/MoS_2 Heterostructured FET

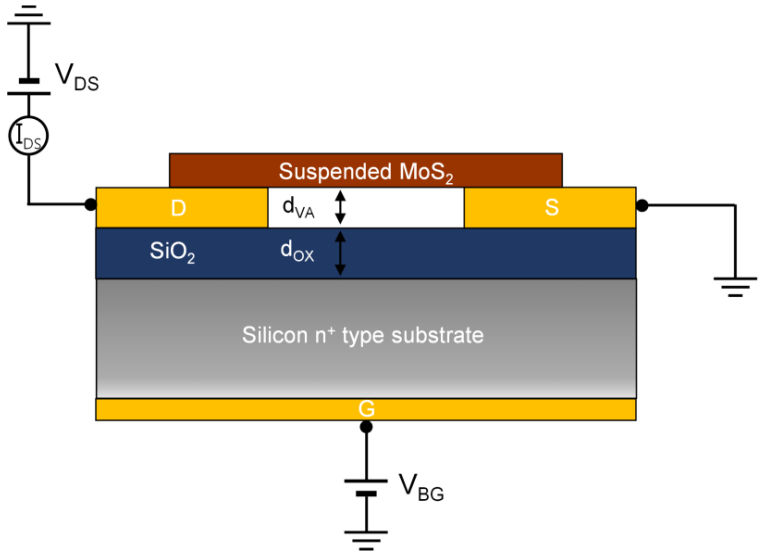


MoS_2/metal interface

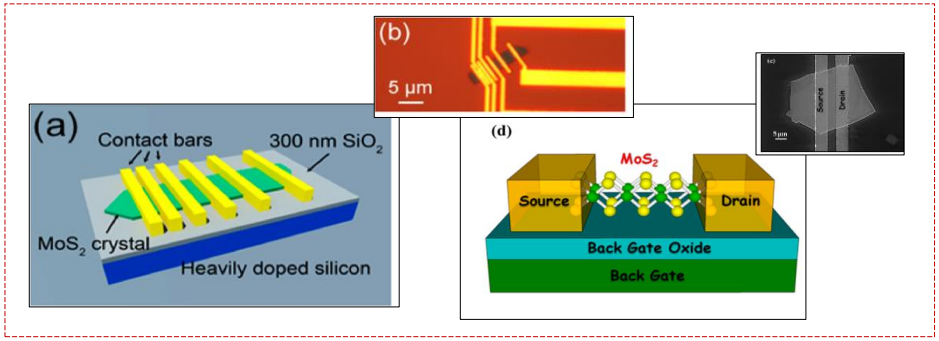
D. Qiu and E. K. Kim, *Scientific Reports* 5, 13743 (2015)

(1) Bridge channel MoS_2 FET

- **Cross-section view of bridge-channel FET**

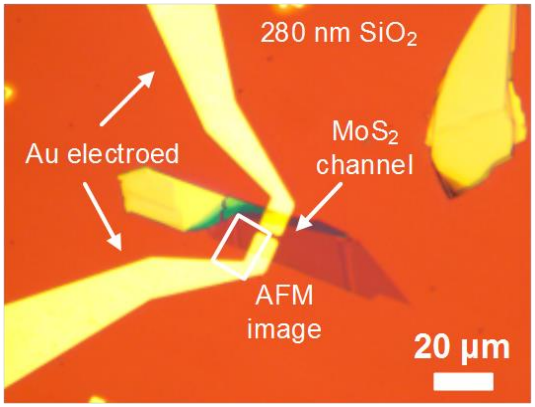


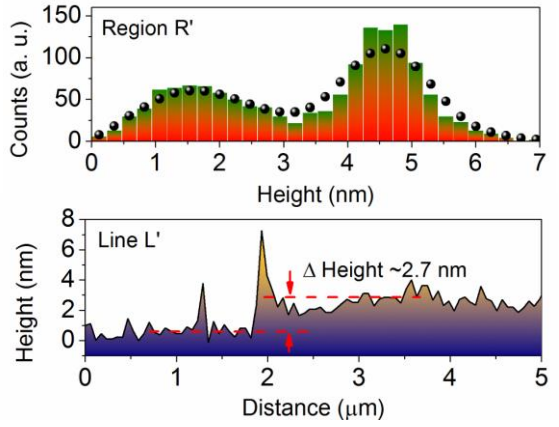
channel length L= 3 μm, width W= 10 μm,
d_{OX}= 280 nm, vacuum gap d_{VA}= 40 nm



The configurations of common top-down device

Optical microscope image

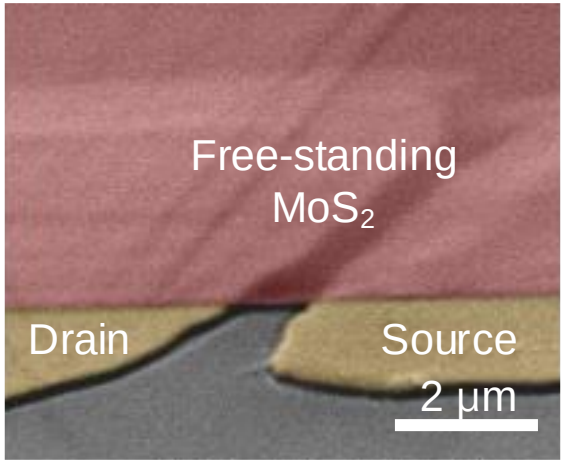


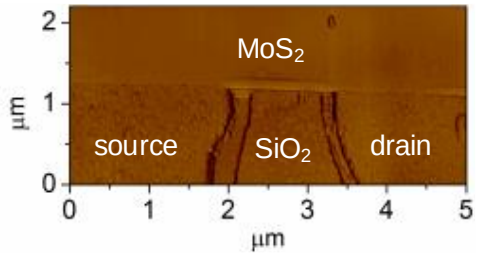


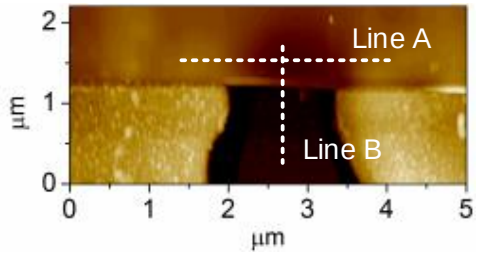
4 layers MoS_2

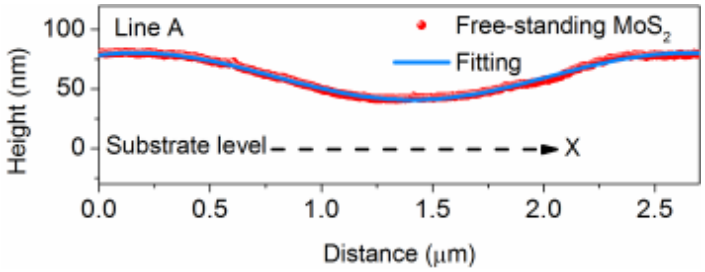
Free standing MoS_2 channel

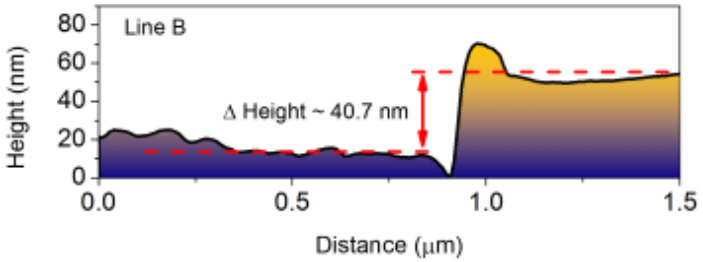
- Tilted angle SEM
- AFM topography
- Height profiles of A and B











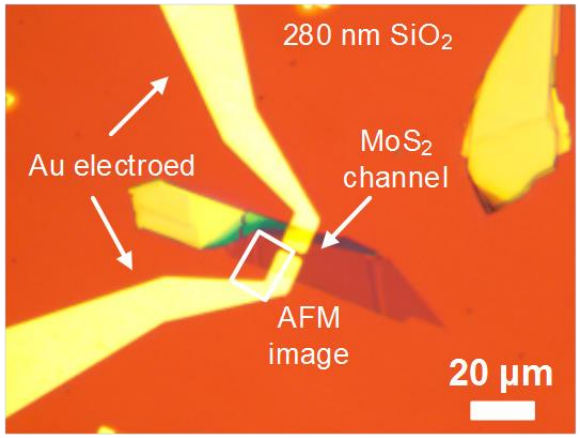
Using the parallel-plate capacitor model the oxide capacitance per unit area is given by $C_{OX} = \varepsilon_r\varepsilon_0/d_{OX}$, and $\varepsilon_0 = 8.854\text{x}10^{14}$ F/m, $\varepsilon_r = 3.9$, $d_{OX} = 280$nm. → $1.23\text{x}10^{-8}$ F/cm^2

And the vacuum capacitance is extracted to be $C_{VA}=1.48\text{x}10^{-8}$ F/cm^2 by calculation with bending profile of MoS_2 bridge.

→ Then the exact total capacitance is $C_{TOT}=7.92\times10^{-9}$ F/cm^2, since oxide capacitor and vacuum capacitor are in series connection.

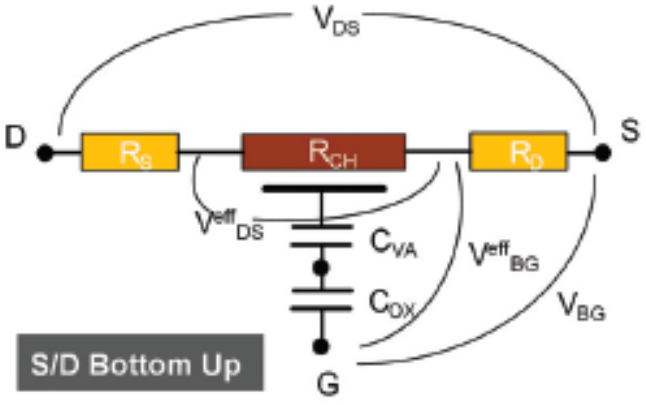
D. Qiu, D. U. Lee, C.-S. Park, K. S. Lee, and E. K. Kim, *Nanoscale,* 7, 17556 (2015)

Electrical characteristics of bridge-channel MoS_2 devices

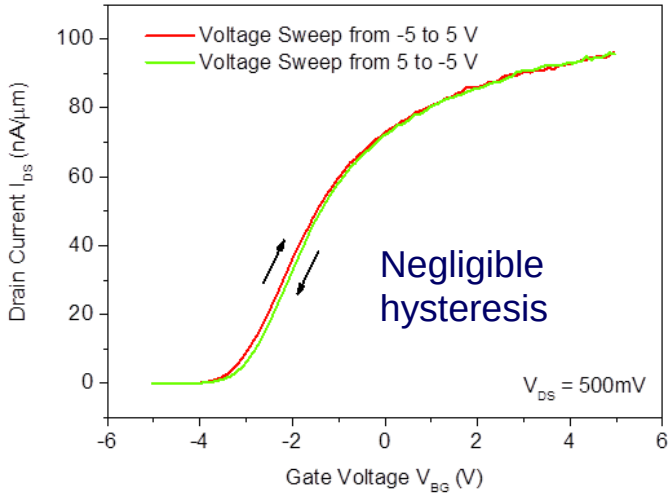


4 layers MoS_2

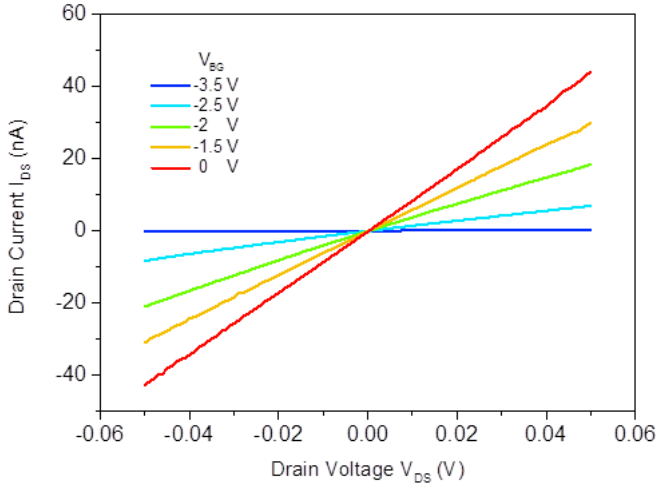
Optical microscope



A circuit model

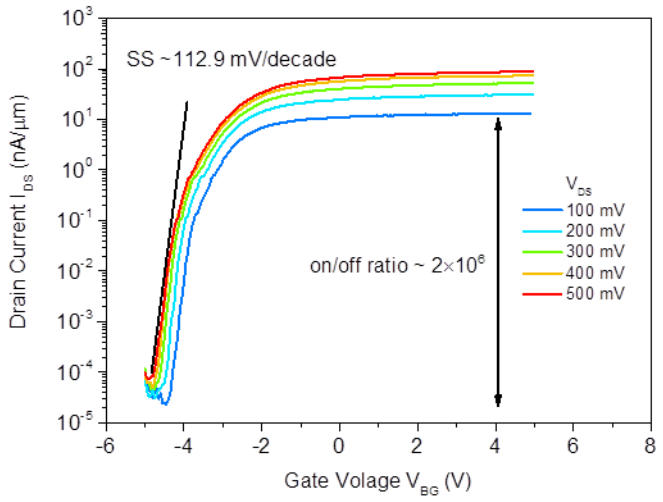


→ Charge trapping centers are negligible.



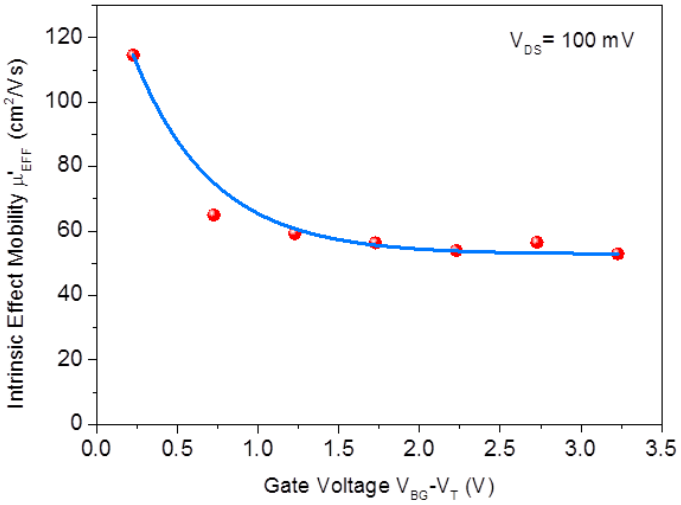
I_{DS}-V_{DS} characteristics at low-bias range → Ohmic

Electrical characteristics



The drain voltage V_{DS} is swept from 100 to 500 mV in 100 mV steps. Typically, the transistors reveal n-type behavior with an average on/off ratio exceeding ~2×10^6 and subthreshold swing of 112.9 mV/decade.

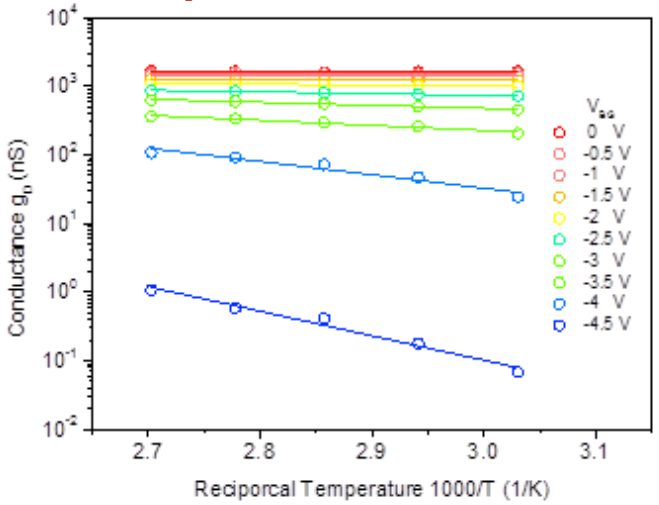
Ref. $SS = \ln(10)(k_BT/e)(1+\eta)$, $\eta = (C_D+C_{IT})/C_{TOT}$

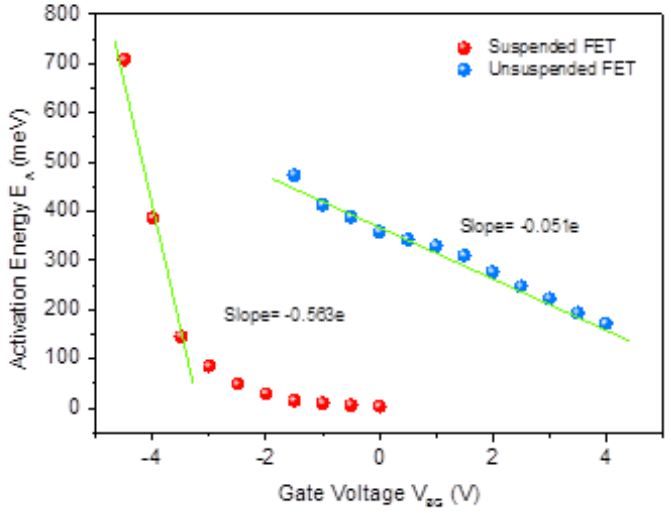


The intrinsic effective mobility of bridge-channel MoS_2 is about 65 $cm^2/V\cdot s$ under low drain bias (V_{DS}= 100 mV) to make FET operating at linear regime. (V_{th} = - 3.2 V)
(cf. μ~12.2 cm^2/Vs on SiO_2)

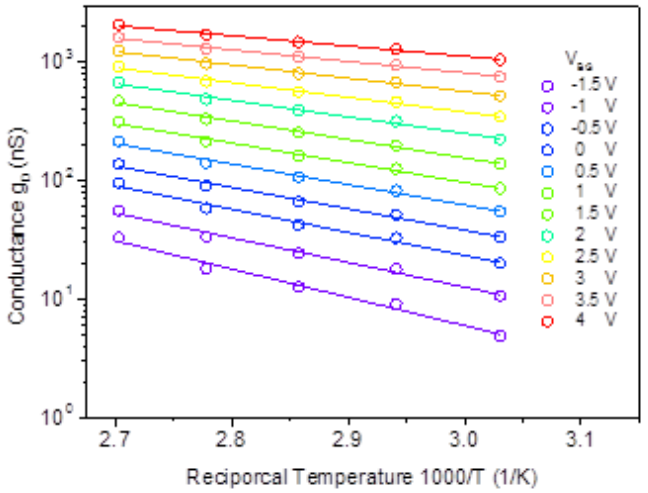
Interface characterization

Suspended device





Unsuspended device



By activation transport model, the conductance

$$g_D = g_0 \exp(-E_A/k_B T)$$

$$D_{IT}(E) = (C_{OX}/e)(dE_A/dV_{BG})^{-1}$$

$dE_F/dV_{BG} = -dE_A/dV_{BG} = 0.563e$, $\quad E_A \approx E_c - E_F$

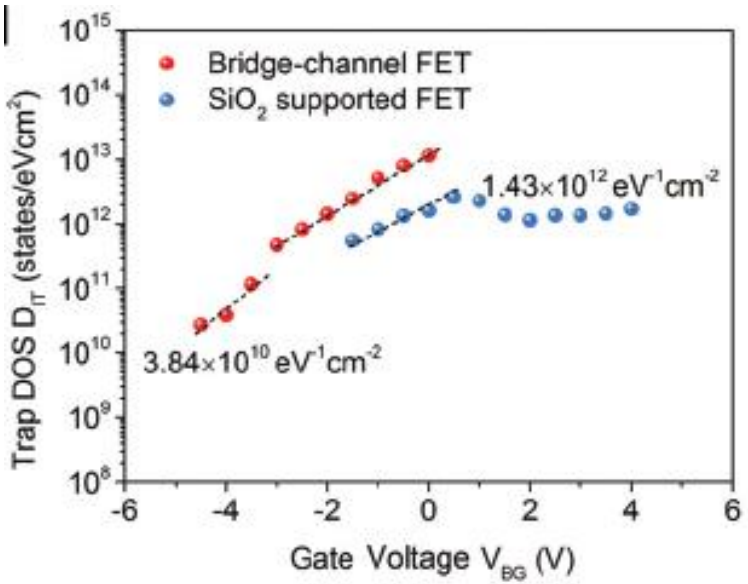
$dE_F/dV_{BG} = eC_{TOT}/(C_{TOT}+C_{IT})$

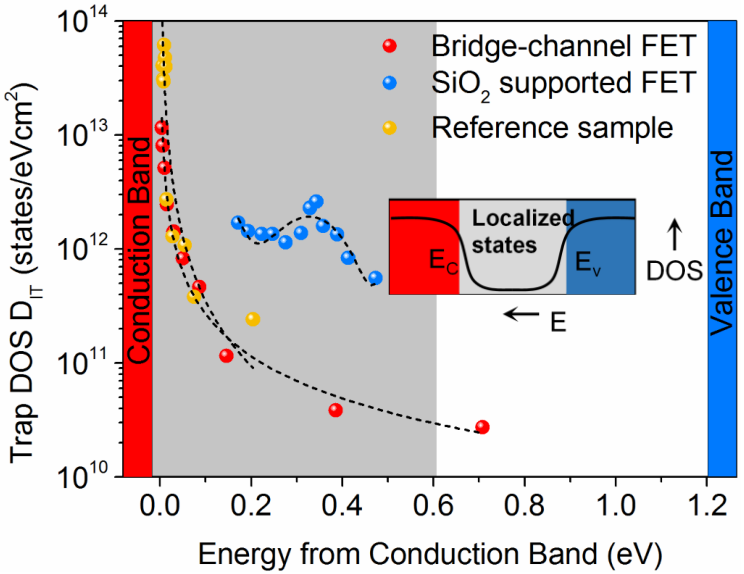
$C_{IT} = e^2 D_{IT}$

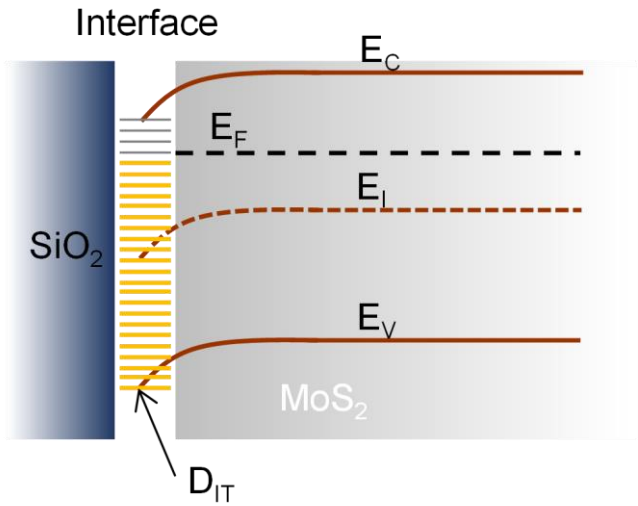
$C_{TOT} = C_{OX}C_{VAC}/(C_{OX}+C_{VAC}) = 7.92\text{x}10^{-9}$ F/cm^2

D_{IT} ➔ 3.84 x 10^{10} states/eVcm^2

Interface characterization







The surface trap DOS of D_{IT}= 3.84 x 10^{10} states/eVcm^2 for bridge-channel FET is two orders of magnitude lower than 1.43 x 10^{12} states/eVcm^2 in the conventional device structure.

Effective mobile charge density is $Q_F \approx C_{OX}(V_{BG}-V_T)\exp(-E_A/k_BT)$.

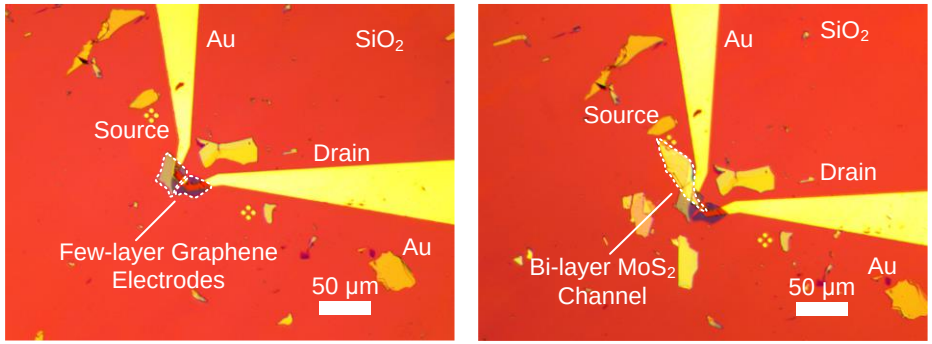
The ratio of effective density mobile charge to total accumulated charge density Q_N at room temperature Q_F/Q_N is only about 0.13% with E_A= 172 meV at V_{BG}= 4V for SiO_2-supported transistors.

For bridge-channel devices, it can be roughly estimated to be 85.8% of injected charge for free with E_A = 3.95 meV at V_{BG}= 0V.

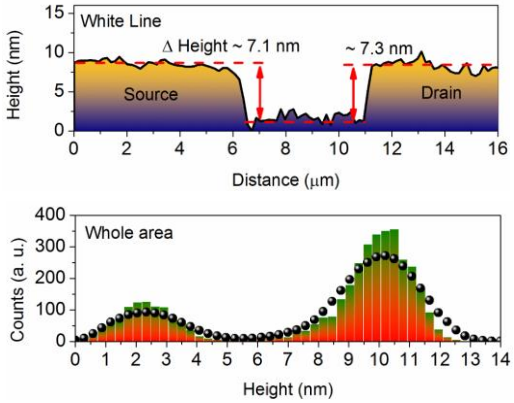
(2) Graphene/MoS_2 Heterostructured FET

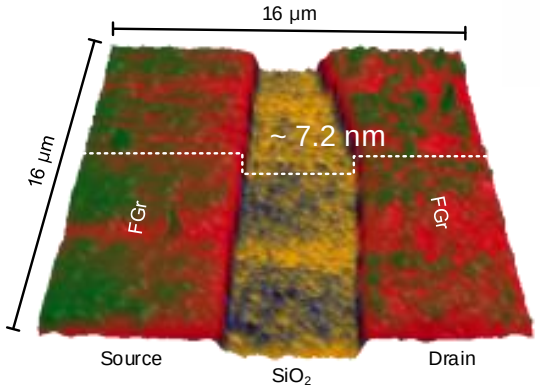
Control of Schottky barrier at metal/MoS_2 contact by inserting of multi-layered graphene

- **Optical microscope image**

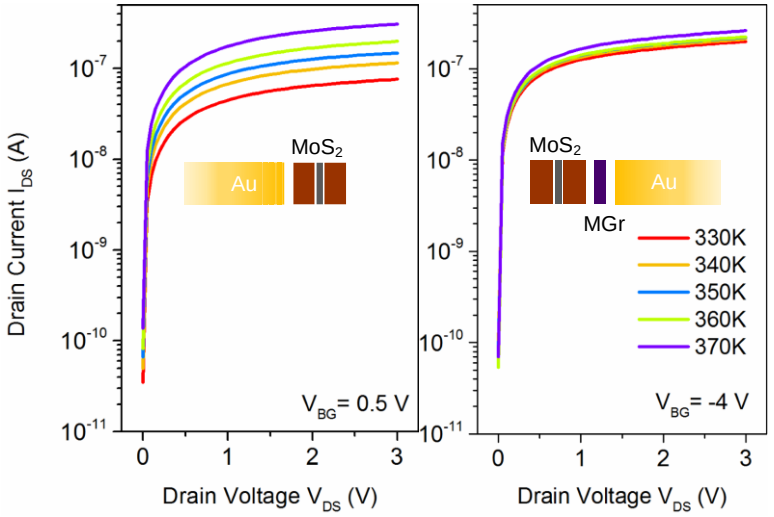


Channel *L*= 3.5μm, *W*= 5.2μm





3D AFM topographic image

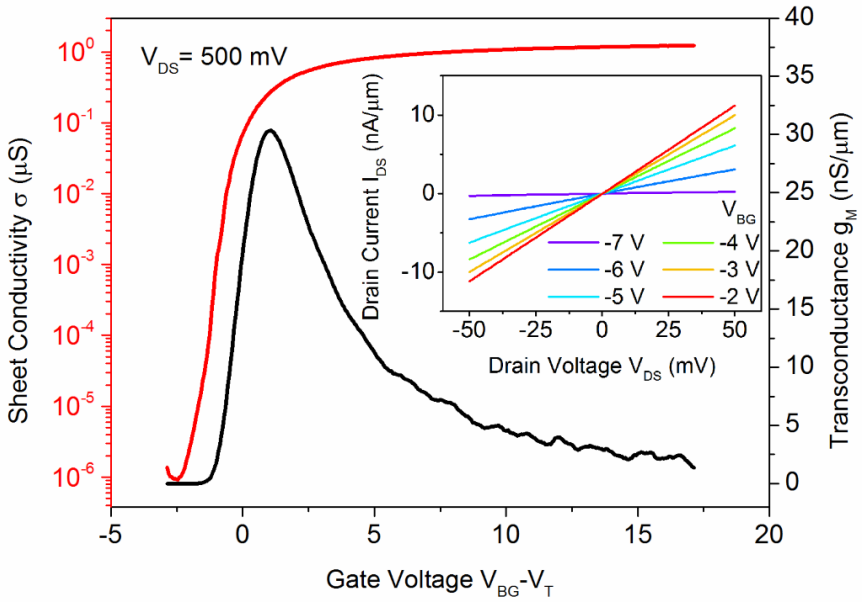


Temp.-dependent I_{DS}-V_{DS} characteristics for an Au/MoS_2 FET (left) and an MGr/MoS_2 FET (right). Temp. ranges from 330 to 370 K.
The inset shows the corresponding device configurations

→ multi-layer graphene could significantly affect the temp. dependent I-V output curves.

D. Qiu and E. K. Kim, *Scientific Reports* 5, 13743 (2015)

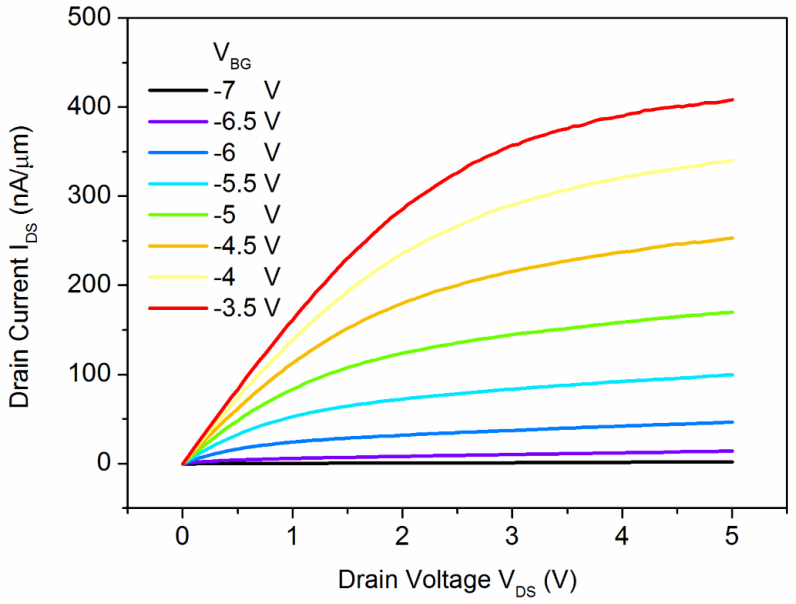
Electrical transport behavior



Normalized *I-V* transfer characteristics of a typical back-gated MGr/MoS_2 device at a fixed drain voltage.→ current on/off ratio of 10^6 and transconductance g_M ~ 30 nS/μm.

Inset: I_{DS}-V_{DS} curve at a low drain bias (V=±50 mV). The linearity was maintained under various gate voltages.

(*Ref.* $g_M = \partial I_{DS}/\partial V_{BG}$)



Output characteristics at various gate voltages

Field-effect mobility of bi-layer MoS_2

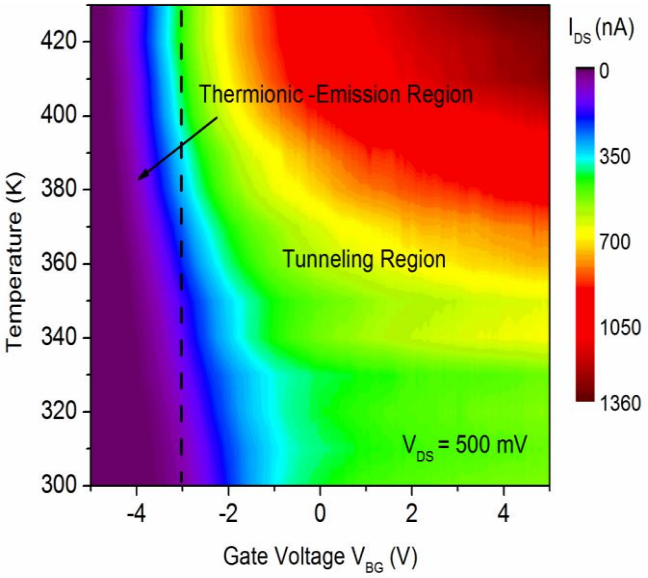
μ_{FE} ~ 17.9 $cm^2/V{\cdot}s$

→comparable to those of mono- or bi-layer MoS_2 in high-*K* gate dielectric capping devices.

$$\mu_{FE} = g_M \left(\frac{L}{W}\right) C_{ox} V_{DS}$$

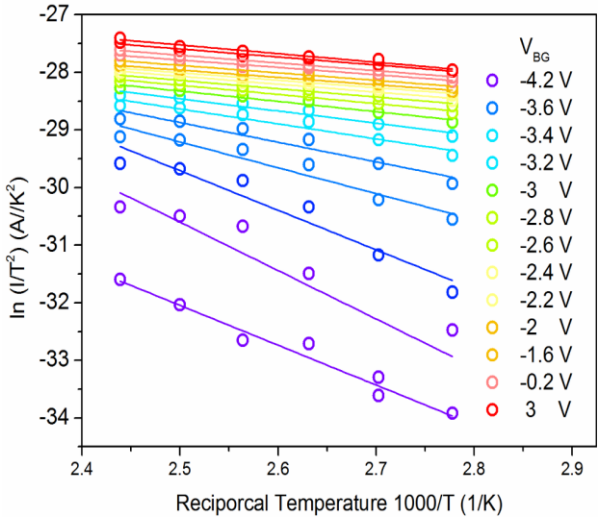
$$C_{ox} = \varepsilon_r \varepsilon_o / d_{ox}$$

Extraction of Schottky barrier height

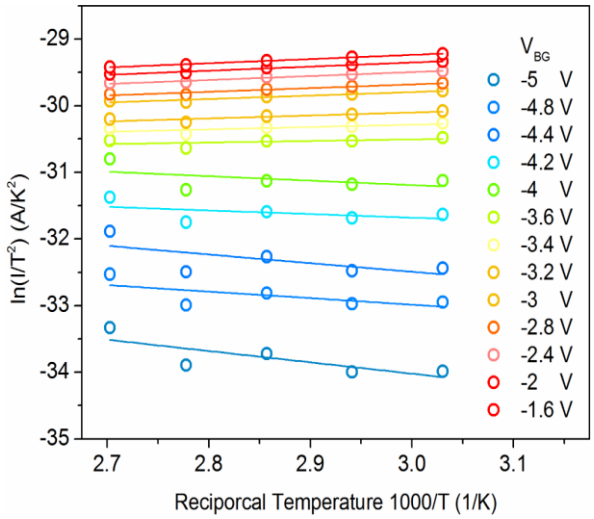


Color map of temperature-dependent transfer characteristics at V_{DS}=500 mV.

Au/MoS_2 FET



MGr/MoS_2 FET



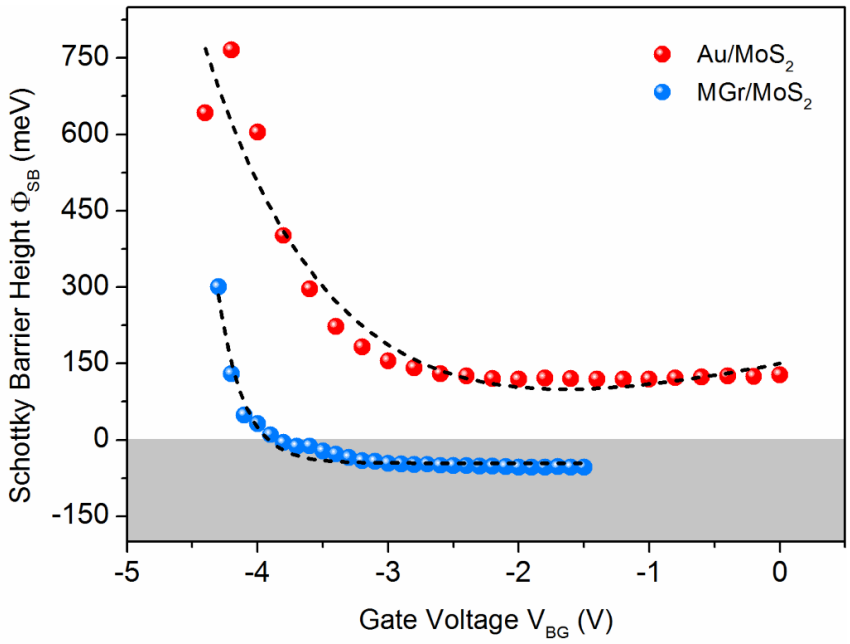
Arrhenius plots of $\ln(I_{DS}/T^2)$ *vs.* $1000/T$ at various gate voltages for MoS_2 FET

Thermionic equation $$I_{DS} = AA^{**}T^2 \exp\left(-\frac{e\emptyset_{SB}}{k_B T}\right)\left[\exp\left(\frac{eV_{DS}}{k_B T}\right) - 1\right]$$

MoS_2 contact with gold electrode displays strong temperature dependence, but MoS_2 with MGr contact displays weak temperature dependence.

For MGr/MoS_2 devices, slope of the linear fit curve in Arrhenius plot is negative near the off-state (V_{BG} ~ -5 V) and becomes more positive with the formation of a highly conductive MoS_2 channel at V_{BG} = −1.6 V.

Negative Schottky barrier behavior

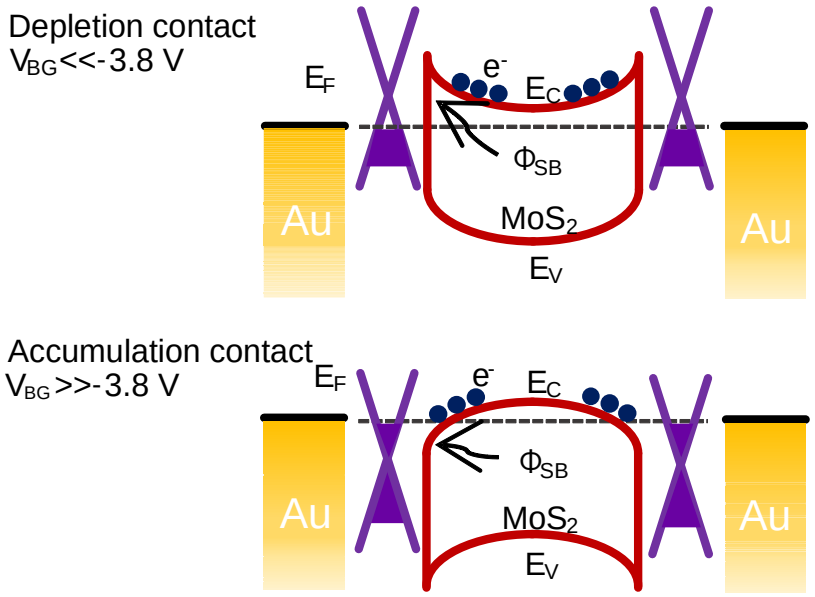


Gate bias dependence of Schottky barrier height.

Φ_{SB} : from 300 to -45.5 meV for MGr/MoS_2

cf) from 765.9 to 111.8 meV for Au/MoS_2

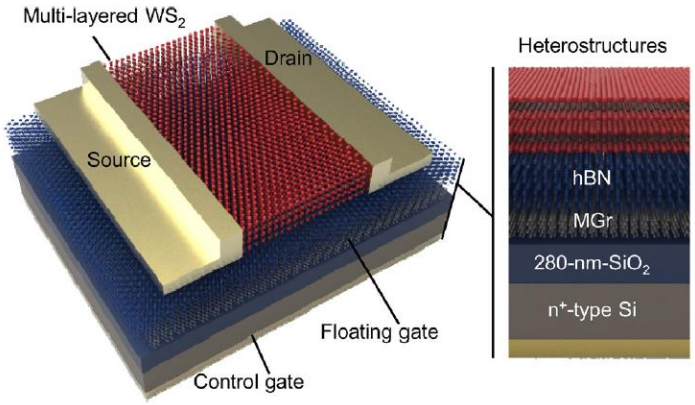
Top: Schematic band diagram for a depletion-type contact.
Bottom: Illustration of an accumulation contact.



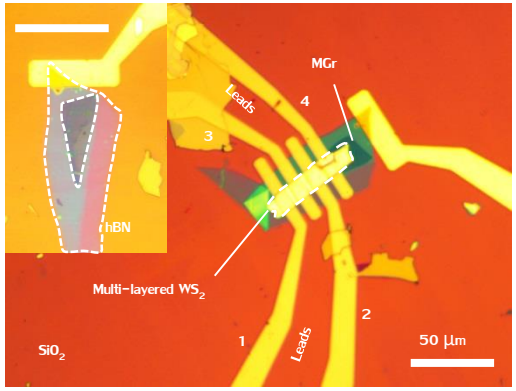
Because Φ_{MGr} depends on the back-gate electric field, the carrier density in the MGr shifts the Fermi level by $\Delta E_{F,MGr}=\hbar v_F[\pi|C_{OX}/e(V_{BG}-V_T)|)]^{1/2}$, where v_F is the Fermi velocity.

The tunable Schottky barrier is primarily responsible for modulation of the work function of thick graphene. Despite the large number of graphene layers, ohmic contacts can be formed.

II. Structure of MGr-embedded memory devices



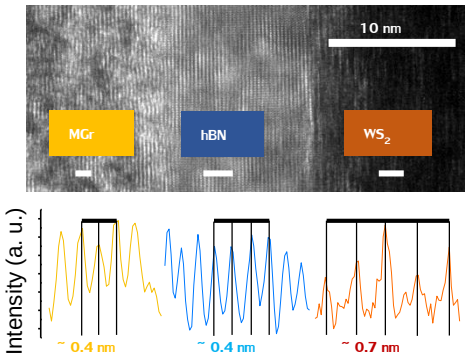
Schematic representation of a 2D crystal stacked memory device.

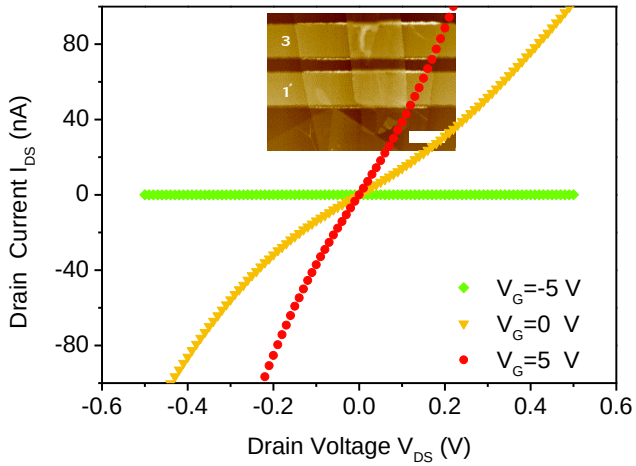


Optical image of a multi-layered WS_2 memory transistor.

Inset: optical image of the device before metallization. The multi-layered graphene encapsulated by hBN flake had a triangular shape for electrical isolation (scale bar: 50 μm).

HRTEM image of WS_2/hBN/MGr

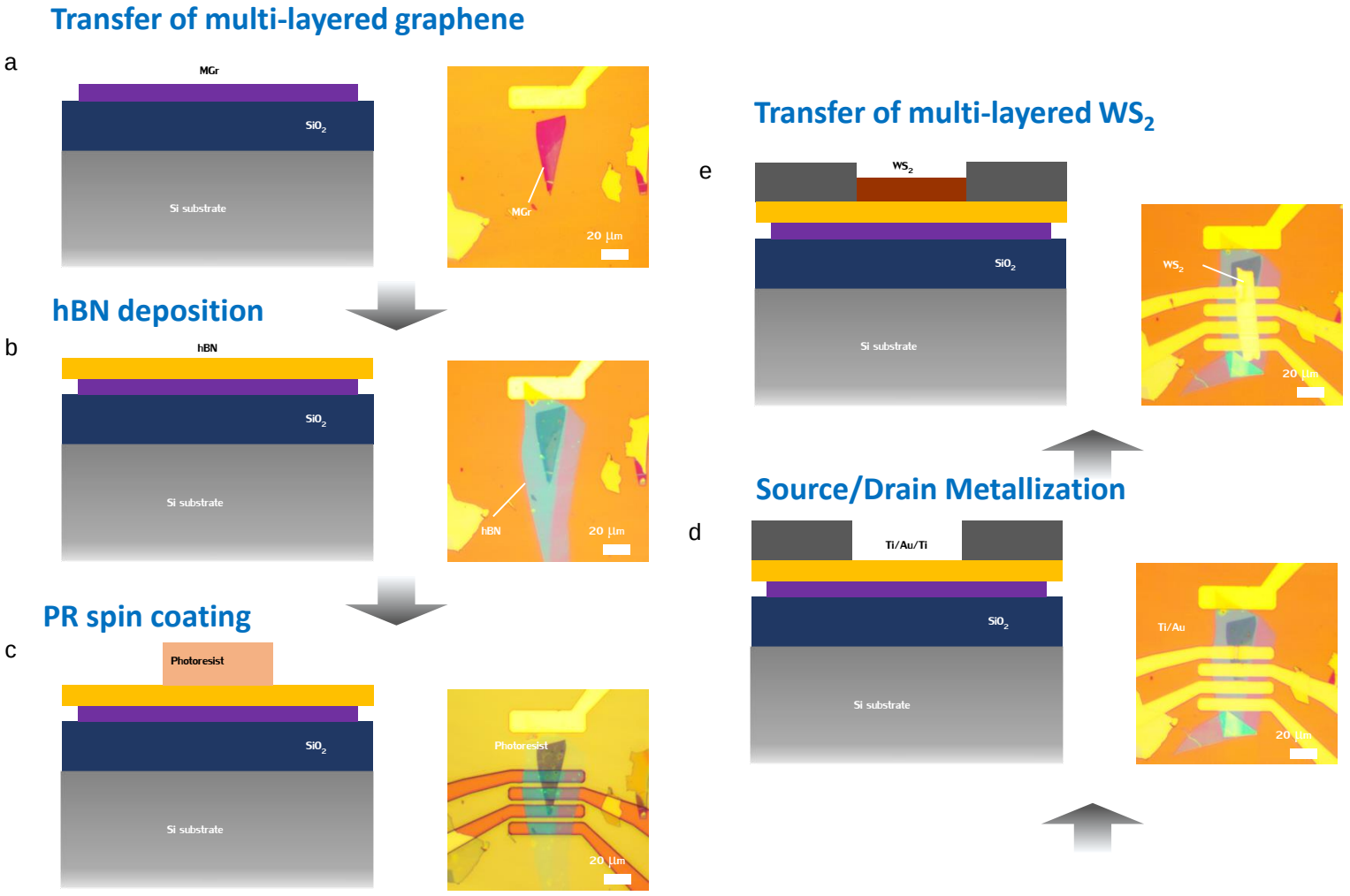




AFM image and Small drain voltage dependence of the current under different gate voltages

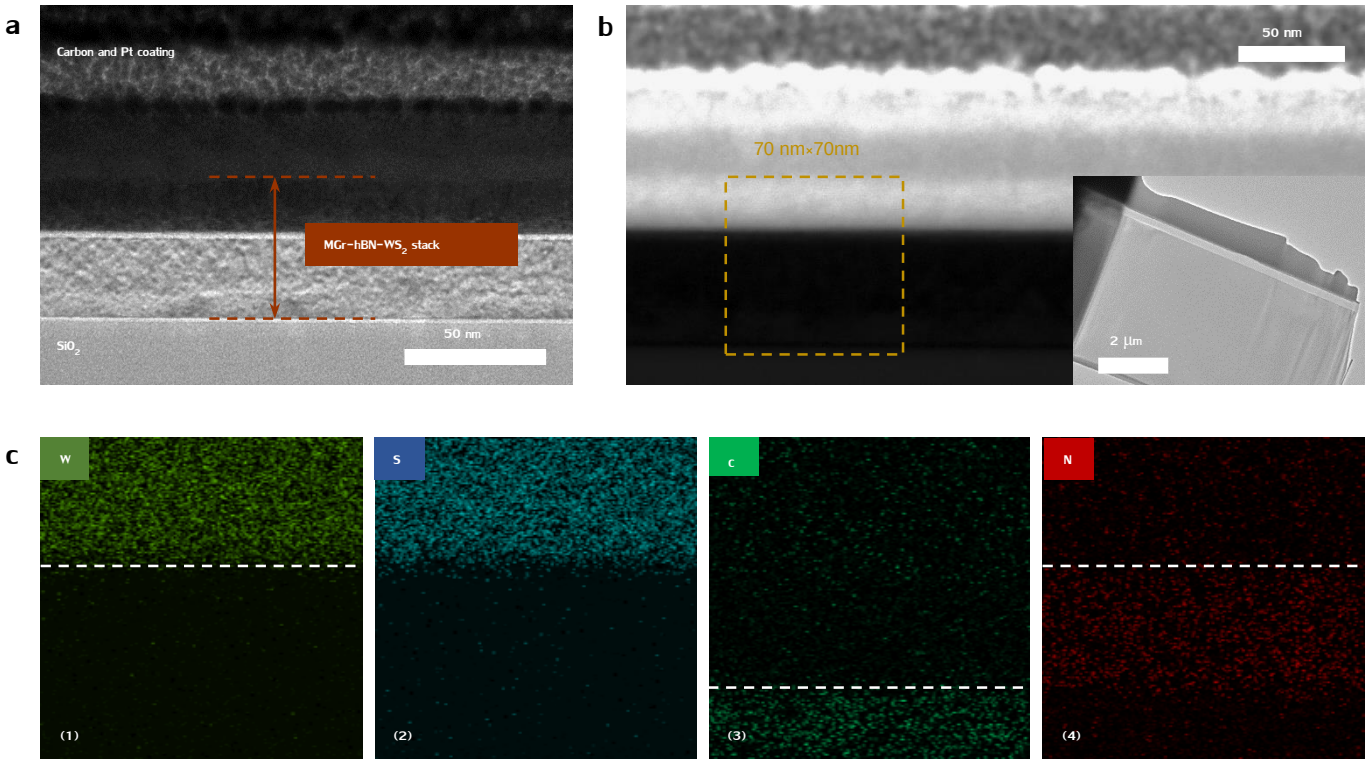
D. Qiu, E.K. Kim *et. al*, Nano Res. 9, 2319 (2016)

Fabrication process for MGr-embedded memory device



D. Qiu, D.U. Lee, K.S. Lee, S.W. Pak, and E.K. Kim, *Nano Res*. 9, 2319 (2016)

Material and structural characterizations

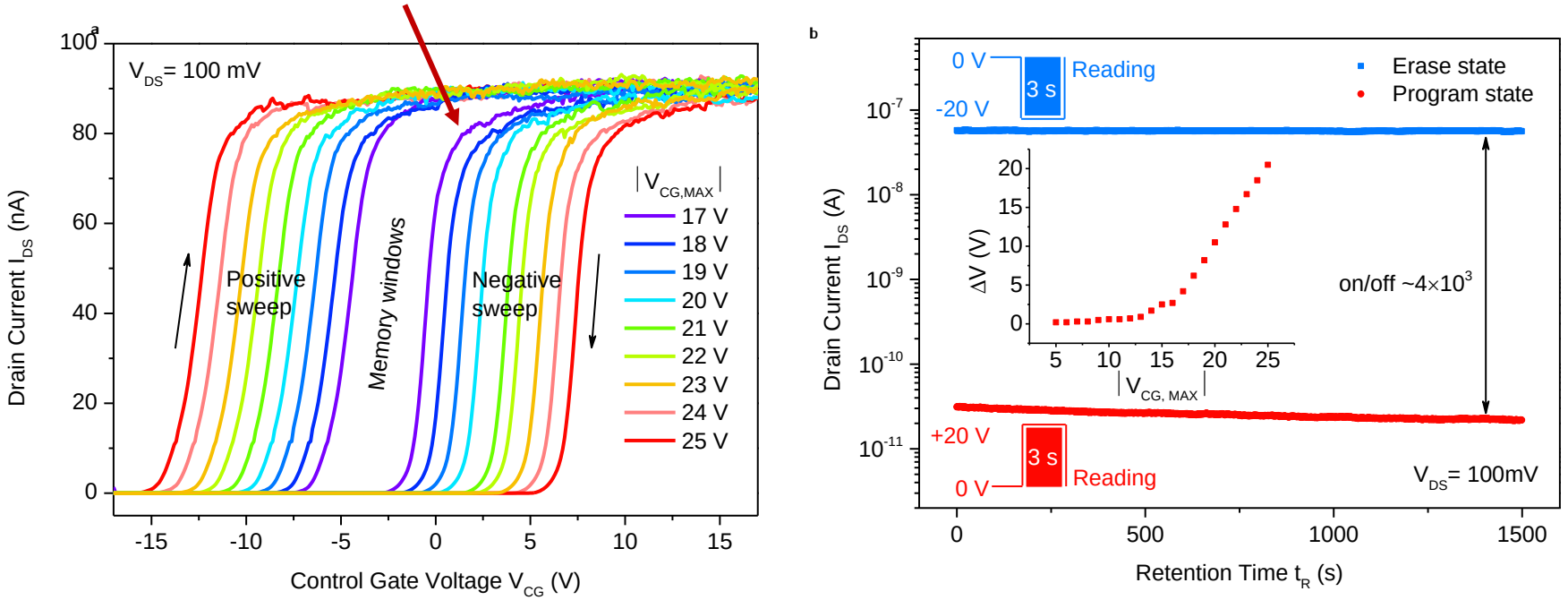


Cross-sectional TEM imaging and EDX mapping of van der Waals heterostructure.
(a) Cross-sectional HRTEM image,
(b) STEM micrograph of a WS_2–hBN–MGr stack. Inset: low magnification TEM image of the final site-specific samples for TEM imaging.
(c) Elemental mapping for W, S, C, and N acquired from the EDX measurement.

Electrical performance

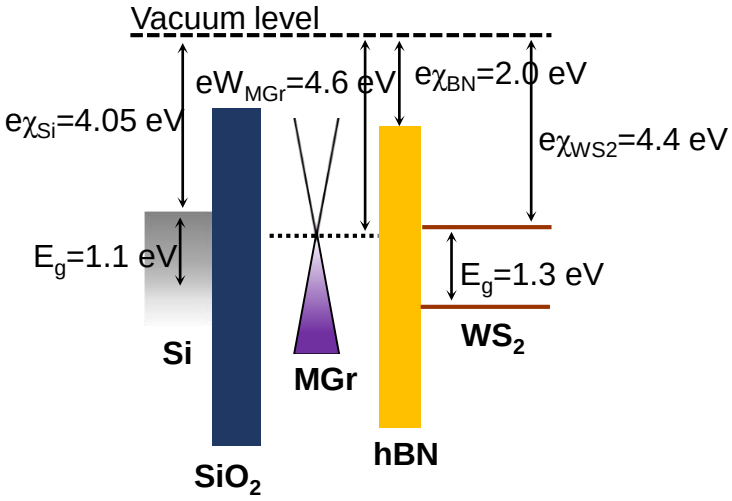
Memory window opening up to 20 V

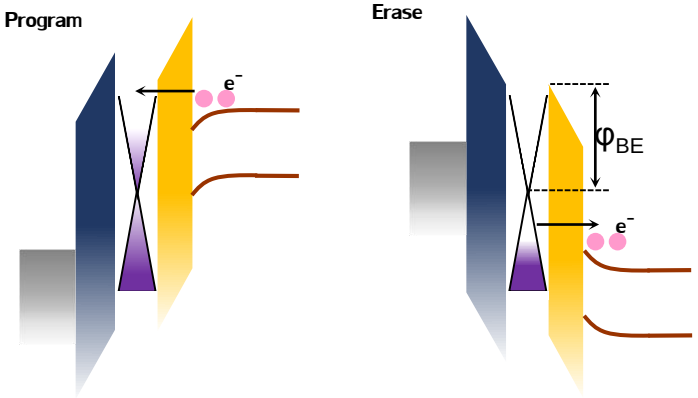
Erase/program ratio >10³



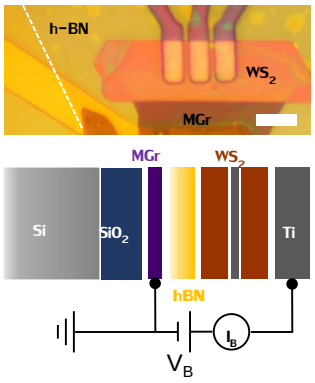
Electrical performance of the memory devices.
(a) I_{DS}–V_{CG} transfer characteristics of the device acquired using positive and negative voltage sweeps at V_{DS} = 100 mV. The maximum control gate voltage changes from 5 to 25 V.
(b) Evolution of temporal retention characteristics after applying ±20 V for a Δt = 3 s pulse with an erase/program state ratio of 4 × 10^3 for a t_R = 1,500 s retention time. Inset: memory window as a function of maximum control gate voltages extracted from data in (a).

Charge trapping & electrical conduction





Energy band diagram of floating-gate memories in the program (V_{CG} > 0) and erase operation (V_{CG} < 0). Here, ϕ_{BE} represents the tunnel barrier.



Top: Optical image of the Ti–WS_2–hBN–MGr–Ti device (the scale bar is 10 μm). The thickness of WS_2 and hBN were 9.4 and 21 nm, respectively.

Bottom: Schematics of the measurement setup for measuring electrical conduction in the hBN barrier. Here, $J_B = I_B/A$, with an active contact area A.

Carrier transport mechanism through a thin hBN

- **Direct tunneling**:
If the voltage drops on the hBN dielectric satisfies $V_{BN}<\phi_{BE}$

- **Fowler–Nordheim (F–N) tunneling**:
If $V_{BN}>\phi_{BE}$, electrons will encounter a triangular barrier

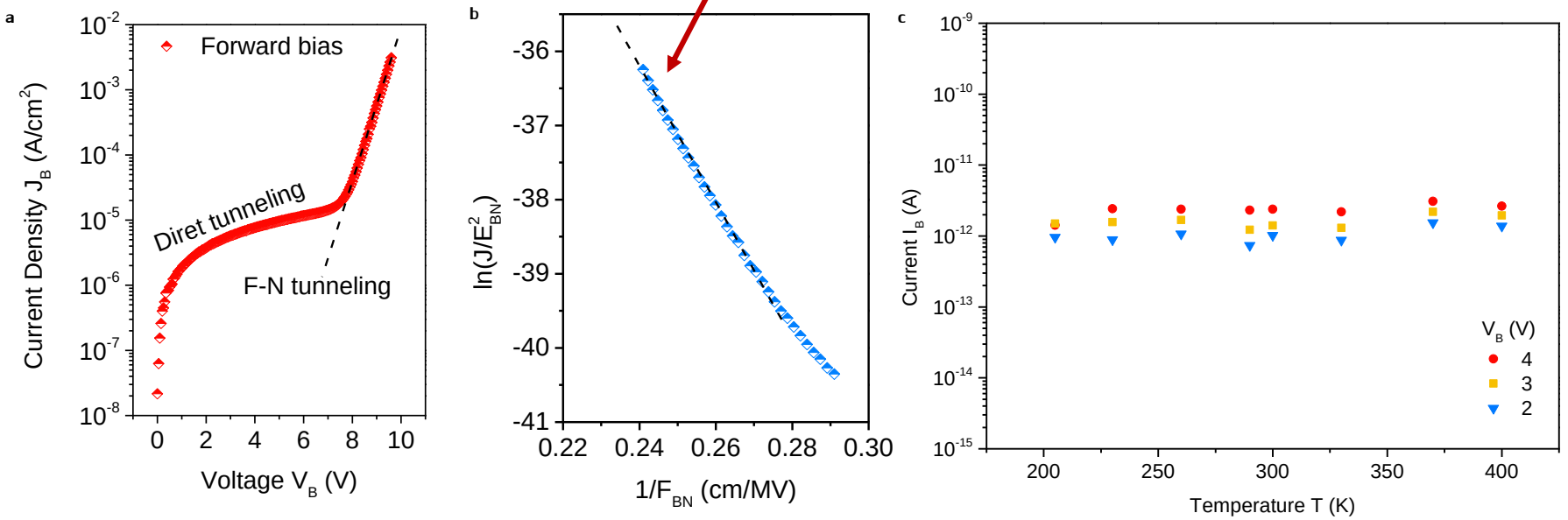
$$J_{FN} = C_1 F_{BN}^2 \exp[-(32\, m_{BN}^*)^{1/2} (e\,\phi_{BE})^{3/2} / 3\hbar e F_{BN}]$$

$$C_1 = e^2 / 16\pi^2 \hbar \phi_{BE} (m_e / m_{BN}^*)$$

where, F_{BN}, $\hbar$, and e are the electric field in the dielectric, Plank's constant, and the elementary charge, respectively

Tunnel barrier extraction

Tunnel barrier is deduced to be 3.0 eV



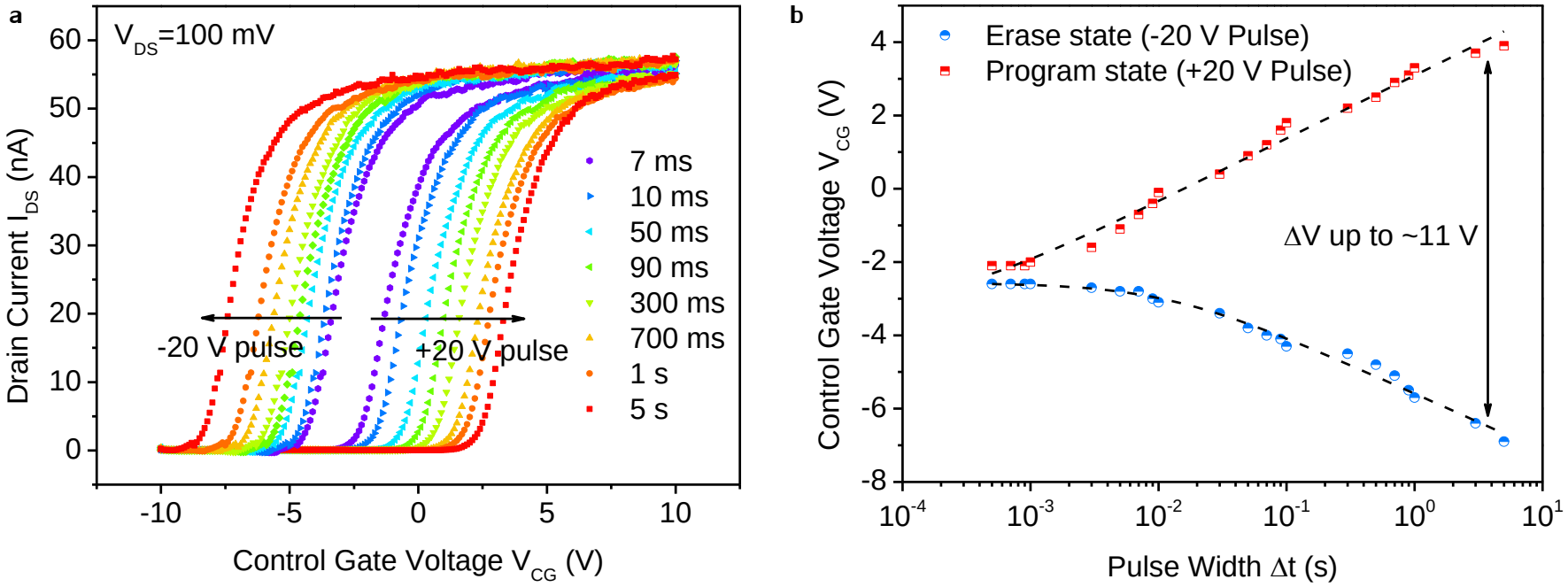
(a) The measured tunneling current density J_B as a function of the applied voltage V_B for the forward direction (positive voltage on WS_2).

(b) F–N plot of the measured current density.→ the tunnel barrier of hBN from graphene was about 3.0 eV.

(c) Temperature dependent I_B–V_B data deduced from V_B = 2–4 V at a temperature range of 200–400 K.

→ The weak temperature dependence of the I_B level indicated that the current across hBN was due to quantum tunneling in the low-bias range.

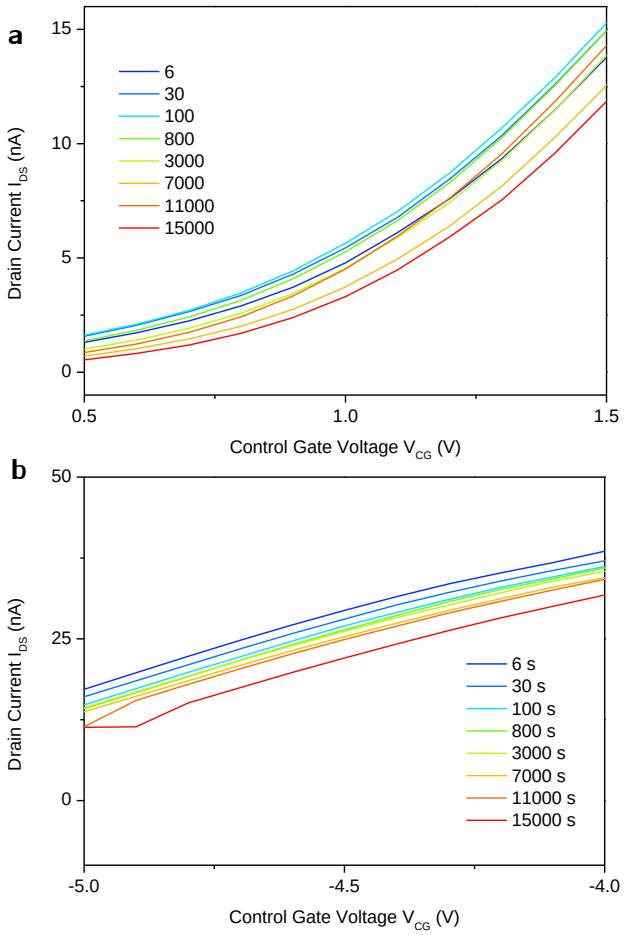
Characteristics of programming and erasing

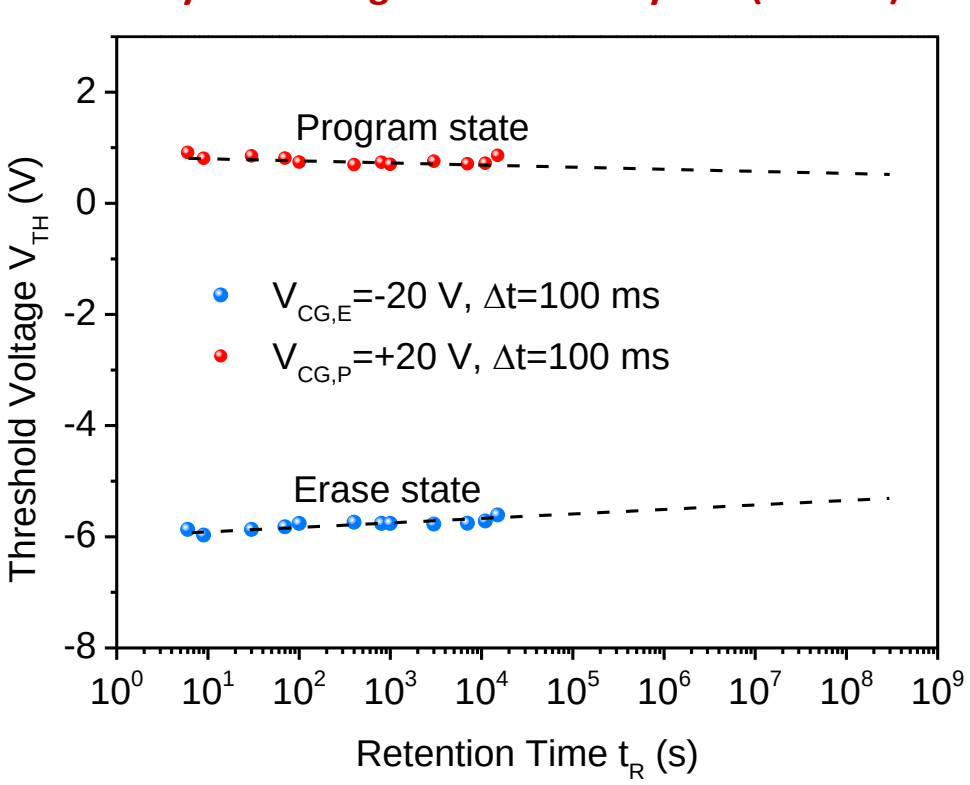


(a) Transient characteristics of the memory device when applying $V_{CG,P}$ = +20 V and $V_{CG,E}$ = −20 V pulses with various width of 7 ms to 5 s.
(b) Separation of relative control gate voltages in the programmed and erased states as a function of the pulse duration time. Data extracted from (a).

The corresponding plot of threshold voltage shift as a function of pulse time can be obtained also.
→ It can be found that long pulse duration results large memory window.

Charge retention characteristics

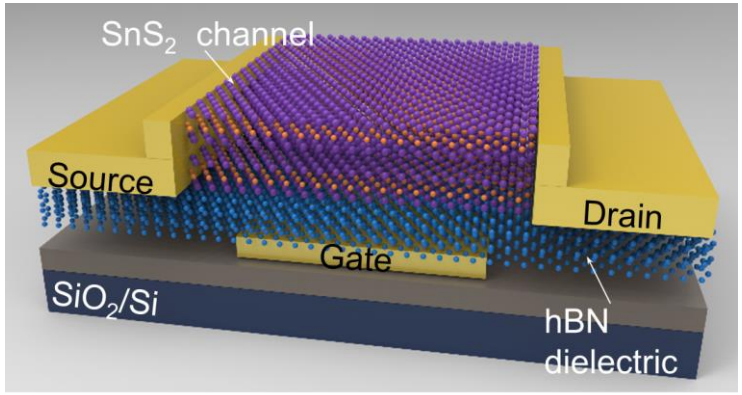




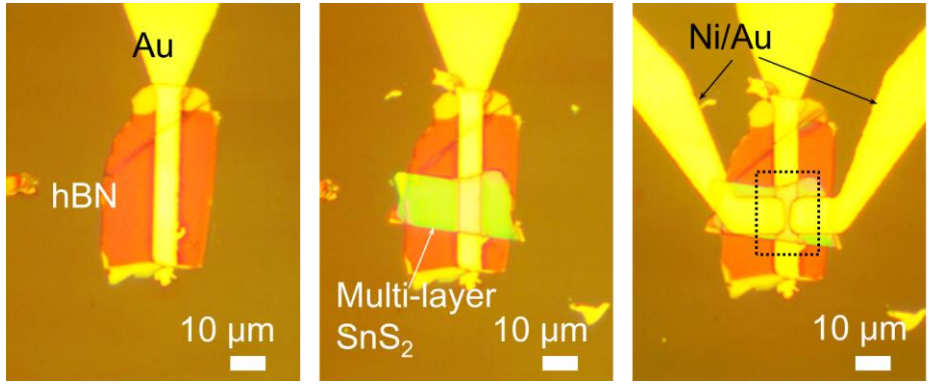
The I_{DS}–V_{CG} transfer curves as a function of retention time at (a) programmed state and (b) erased state for V_{TH} extraction. (c) Charge-retention properties in each state after performing ±20 V, Δt = 100 ms pulses.

→ By linear fitting the V_{TH} for both states, it was retained ~87% of the initial charge on the floating gate after 10 years. It is comparable to the performance of silicon-based ploy-Si floating-gate cells.

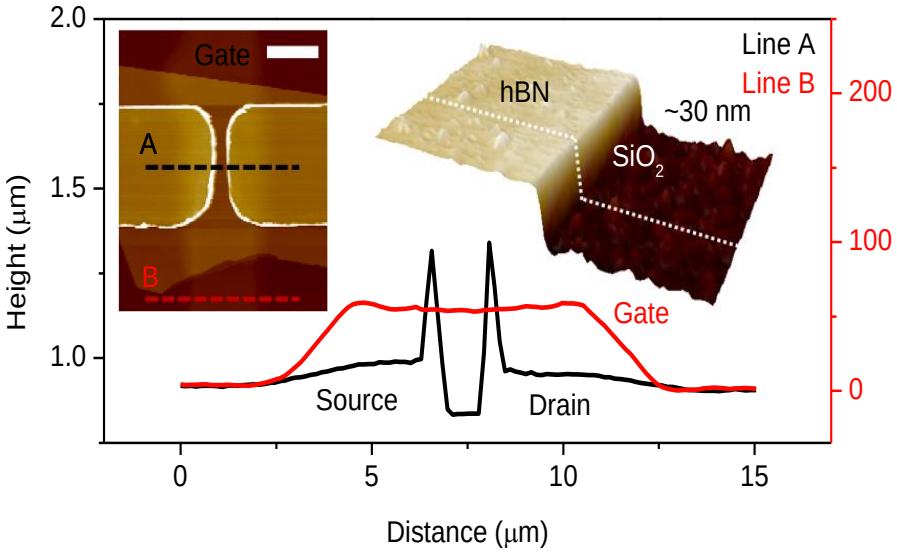
III. SnS_2/hBN TFT with broadband photoresponse



Bottom-gated SnS_2/hBN heterostructure Tr. with gate length/width of 1.5/5 μm



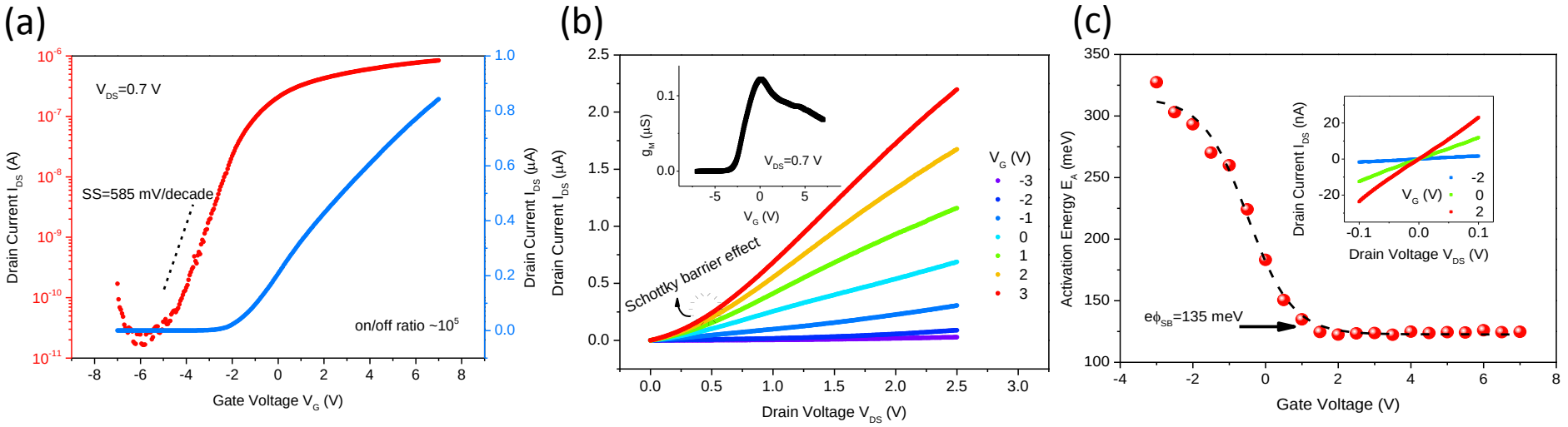
Optical image of hBN flake on gold gate (left), the transfer layered SnS_2 onto top of hBN (middle), and the defined metal leads for source/drain contact (right).



The height profile for line A and B that acquired from AFM image (inset, left) of the device.
The scale bar is 5 μm.
Inset(right): 3D topography for hBN on SiO_2, showing about 30 nm of thickness.

D. Qiu, S. W. Pak, and E. K. Kim, *Scientific Reports* **8**, 10585 (2018)

Electrical transport properties of SnS_2 TFT



(a) Semi-log (left axis, red) and linear (right axis, blue) scale I_{DS}-V_G transfer characteristics of multi-layered SnS_2 transistor biased at V_{DS}= 0.7 V.

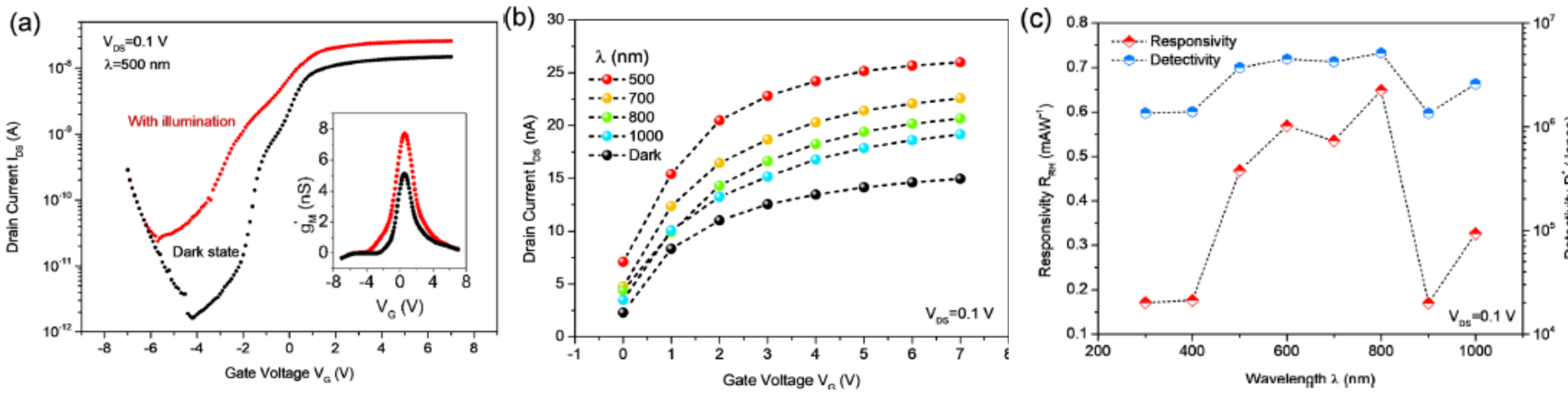
→ The device performed a SS as low as 585 mV/decade and on/off ratio about 10^5 at room-temp.

(b) I_{DS}-V_{DS} output curves for various applied gate bias from -3 to 3 V.
The black circle reveals a non-linear property.
Inset: transconductance vs. bottom-gate voltage at V_{DS}=0.7 V → maximum g_M peak of 0.12 μS.

(c) The extracted activation energy as function of applied gate voltage.
Inset: I-V characteristics under small V_{DS} bias.

→ The Schottky barrier height is evaluated to be 135 meV for Ni/SnS_2 interface.

Photoresponse and responsivity of SnS_2 transistor



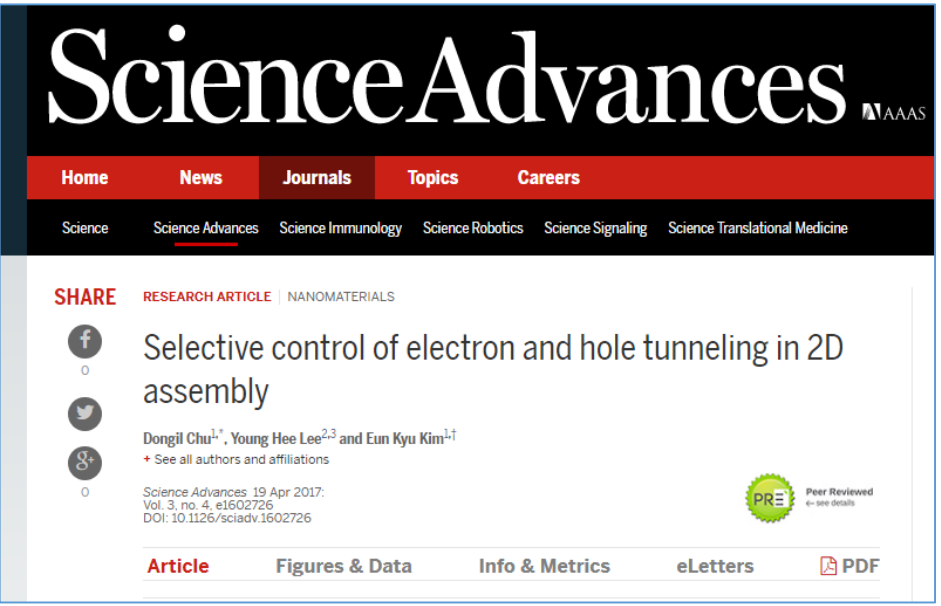
(a) Semi-log I_{DS}-V_G characteristics of the SnS_2 based transistor for dark state and 500 nm wavelength illumination at V_{DS}=0.1 V. Inset: the normalized field effect mobility as a function of gate voltage. The black and red data are corresponding to dark and with illumination condition, respectively.
→ mobility enhancement appears up to 150 %.

(b) Linear scale of transfer curves for different wavelengths (ranging from 500 nm to 1000 nm) under accumulation regime.
→ The device performance exhibits an R_{PH} of 0.47–0.65 mA/W at the visible light range.

(c) Photoresponsivity and detectivity of the device as a function of wavelength at V_{DS}=0.1 V.
→ A maximum R_{PH} of 0.65 mA/W and detectivity in a range of 1.4×10^6 to 5.1×10^6 Jones at V_{DS}=0.1 V and V_G=7 V.

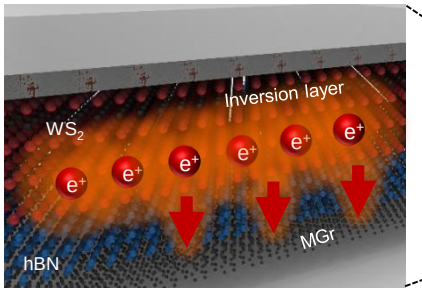
[Jones : cmHz$^{1/2}$/W]

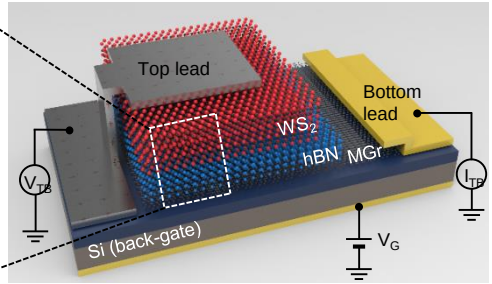
IV. A new conceptual device, CARRISTOR

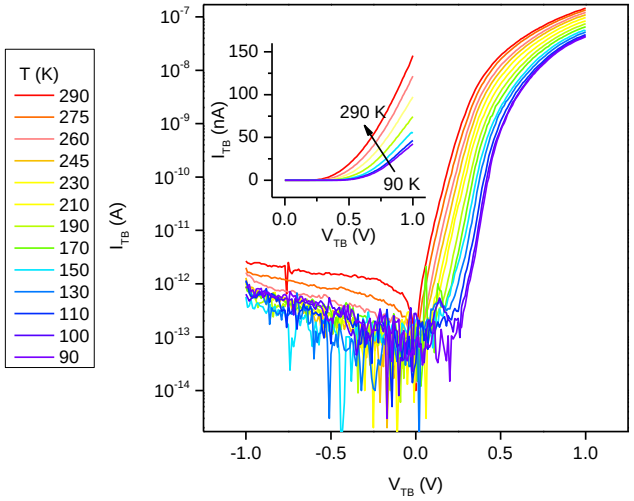


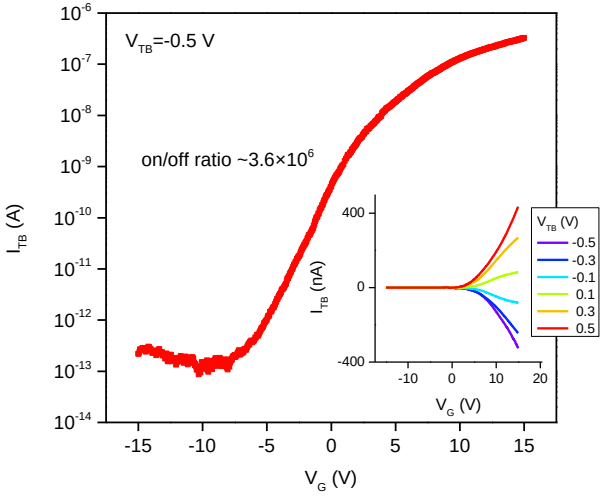
D. Qiu, Y. H. Lee, and E. K. Kim, *Science Advances* **3**(4), e1602726 (2017)

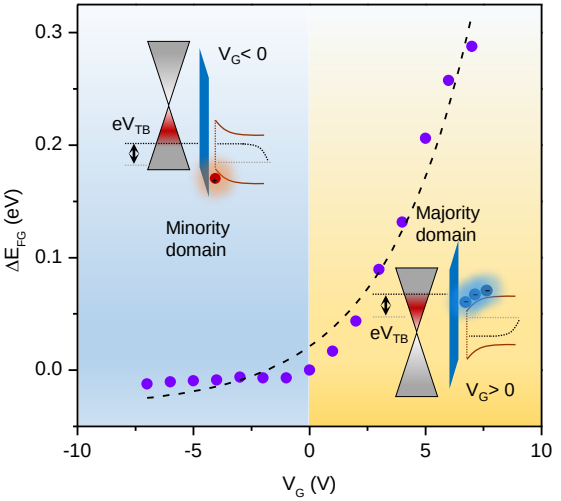
Carristor configuration











Summary

- **We have studied an interface engineering for MoS2 FET.**
  - **Bridge channel FET** with four layer MoS_2 was fabricated and characterized; carrier mobility of about 65.8 cm^2/Vs, on/off ratio of ~2×10^6, SS of 113 mV/decade, and ultra-low trap density of 3.84 x 10^{10} states/$eVcm^2$
  - **Back-gate tunable Schottky barrier** in multi-layered graphene/MoS_2 FET was demonstrated; Schottky barrier height tunable ranges from 300 to -46 meV

- **MGr-embedded nonvolatile memories with WS_2 as a semiconducting channel was produced;** a memory window up to 20 V with a high current ratio around 10^3, perfect charged retention at 13% charge loss after 10 years

- **We demonstrated the SnS_2/hBN heterostructured transistor with a current on/off ratio of ~ 10^5 and SS value of 585 mV/decade, which showed also high photo responsivity of approximately 0.65 mA/W.**

- **We suggested a new conceptual device, CARRISTOR, which is a carrier-type controllable device.**